WHAT IS CLAIMED IS:

1. A method for manufacturing an electronic device which comprises an electronic element having a functional portion and terminal electrodes on a primary surface thereof, and a bond substrate having bond electrodes, which correspond to the terminal electrodes, on a primary surface of the bond substrate, the primary surface of the electronic element facing the primary surface of the bond substrate, the terminal electrodes being bonded to the bond electrodes with bumps provided therebetween for electrical conduction, the electronic element being bonded to the bond substrate with a sealing frame provided therebetween, the sealing frame surrounding the functional portion and the bumps to hermetically seal the electronic device, the method comprising the steps of:

forming a first resist pattern on one of the primary surfaces of the electronic element and the bond substrate, the first resist pattern having openings at locations corresponding to those at which the bumps and the sealing frame are to be formed;

sequentially forming metals over the first resist pattern, the metals being formed into at least one adhesion layer, at least one barrier metal layer, and at least one solder layer;

removing the first resist pattern such that the bumps and the sealing frame are simultaneously formed on said one of the primary surfaces of the electronic element and the bond substrate;

forming a metal layer, which faces the sealing frame, on the primary surface other than said one of the primary surfaces of the electronic element and the bond substrate; and

bonding the electronic element and the bond substrate to each other with the bumps and the sealing frame provided therebetween, in which the solder layer is heated such that metals forming the solder layer are alloyed or the solder layer is alloyed with a metal layer adjacent thereto to form metal bonding.

2. The method for manufacturing an electronic device according to Claim 1, wherein the step of forming the metal layer, which faces the sealing frame, on said primary surface other than said one of the primary surfaces of the electronic element and the bond substrate, comprises the steps of:

forming a second resist pattern on said primary surface other than said one of the primary surfaces of the electronic element and the bond substrate, the second resist pattern having openings at locations corresponding to those at which the bumps and the sealing frame are to be formed;

sequentially forming metals over the second resist pattern, the metals being formed into at least one adhesion layer, at least one barrier metal layer, and at least one solder layer; and

a step of removing the second resist pattern such that the metal layer used as a sealing frame is formed on said primary surface together with bumps.

3. The method for manufacturing an electronic device according to Claim 2, wherein the width of the sealing frame formed on the primary surface of the electronic element is different from that of the sealing frame formed on the primary surface of the bond substrate, and the thickness of the barrier metal layer forming the sealing frame having a smaller width is larger than that of the barrier metal layer forming the sealing frame having a larger width.

4. The method for manufacturing an electronic device according to Claim 1, wherein the solder layer includes Sn as a primary component and at least one metal selected from the group consisting of Au, Ag, Cu, Zn, Si, Ge, Pb, In, Bi, and Sb;

said at least two metals which form the solder layer are deposited to form a layered structure; and

the solder layer having the layered structure including said at least two metals is alloyed by heating.

5. The method for manufacturing an electronic device according to Claim 1, wherein the solder layer includes Sn, the barrier metal layer includes one of Au, Ag, Ni, and Cu, and the solder layer is alloyed with a portion of the metal forming the barrier metal layer by heating the solder layer.

6. The method for manufacturing an electronic device according to Claim 1, wherein the electrodes and the metal layer facing the bumps and the sealing frame, respectively, have surface portions each of which includes one metal selected from the group consisting of Au, Ag, Ni, and Cu, and the solder

layers are alloyed with the metal of the surface portions of the electrodes and the metal layer by heating the solder layers.

7. The method for manufacturing an electronic device according to Claim 1, wherein the at least one adhesion layer is made of Ti, the at least one barrier metal layer is made of Ni, and the at least one solder layer includes Sn as a primary component and Cu.

8. The method for manufacturing an electronic device according to Claim 7, wherein the at least one adhesion layer has a thickness of about 50 nm, the at least one barrier metal layer has a thickness of about 1.2 μm, and the at least one solder layer has a thickness of about 20 μm.

9. The method for manufacturing an electronic device according to Claim 1, wherein the step of bonding the electronic element and the bond substrate to each other is performed at a temperature of about 260°C.

10. The method for manufacturing an electronic device according to Claim 9, wherein the step of bonding the electronic element and the bond substrate to each other is performed in a nitrogen atmosphere containing oxygen at a concentration of about 100 ppm.

11. The method for manufacturing an electronic device according to Claim 1, wherein the at least one solder layer includes an Ag layer, an Sn layer and an Au layer.

12. The method for manufacturing an electronic device according to Claim 11, wherein the Ag layer has a thickness of about 0.5 μm, the Sn layer

has a thickness of about 20 μm, and the Au layer has a thickness of about 0.1 μm.

13. The method for manufacturing an electronic device according to Claim 11, wherein the step of bonding the electronic element and the bond substrate to each other includes the step of heating the at least one solder layer to at least about 232°C such that the Ag layer is dissolved in the Sn layer to form an SnAg solder alloy.

14. The method for manufacturing an electronic device according to Claim 1, wherein the at least one solder layer includes an Ag layer, an Sn layer and an Au layer which are sequentially formed.

15. The method for manufacturing an electronic device according to Claim 1, wherein the at least one adhesion layer is made of Ti, the at least one barrier metal layer is made of Cu, and the at least one solder layer includes Cu_3Sn as a primary component.

16. The method for manufacturing an electronic device according to Claim 15, wherein the at least one solder layer includes at least about 39 percent by weight of Cu.

17. The method for manufacturing an electronic device according to Claim 1, wherein the step of bonding the electronic element and the bond substrate to each other is performed at a temperature of about 280°C for about 60 seconds at a pressure of about 0.5 MPa.

18. The method for manufacturing an electronic device according to Claim 1, wherein the electronic element is a surface acoustic wave element.

19. The method for manufacturing an electronic device according to Claim 1, wherein the electronic element is a bulk acoustic wave element.